1.Features

- Embedded EEPROM
  - Very Easy Development with RFPDK
  - All Features Programmable
- Frequency Range:
  - 240 to 480 MHz
- OOK Modulation
- Output Power: -10 to +13 dBm
- Supply Voltage: 1.8 to 3.6 V
- Current Consumption: 23 mA @ +10 dBm
- Sleep Current: < 20 nA
- FCC / ETSI Compliant
- RoHS Compliant
- Symbol Rate: 0.5 to 30 ksps

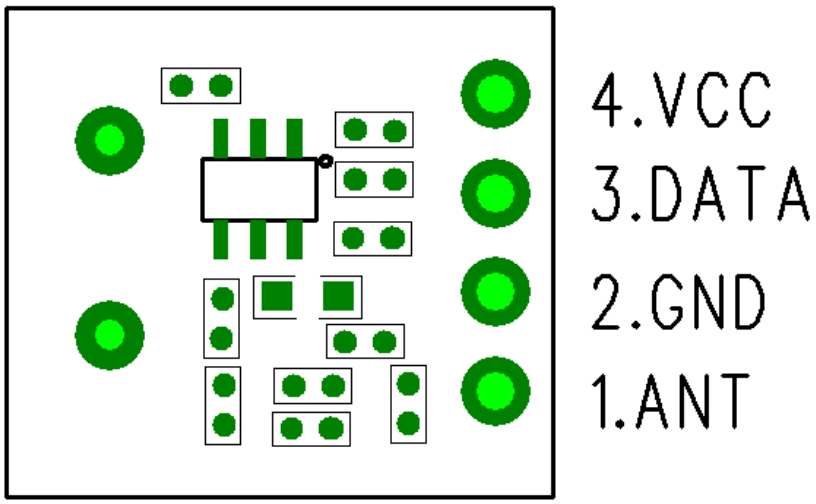
2.Applications

- Low-Cost Consumer Electronics Applications
- Home and Building Automation
- Remote Fan Controllers
- Infrared Transmitter Replacements
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Remote Keyless Entry (RKE)

3.Descriptions

The HCT109 devices are ultra low-cost, highly flexible, high performance, single-chip OOK transmitters for various 240 to 480 MHz wireless applications. They are part of the CMOSTEK NextGenRF^{TM} family, which includes a complete line of transmitters, receivers and transceivers. With very low current consumption, the device modulates and transmits the data which is sent from the host MCU. An embedded EEPROM allows the frequency, output power and other features to be programmed into the chip using the stock products of 315/433.92 MHz are available for immediate demands without the need of EEPROM programming. The HCT109 uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components.

4. Pin Descriptions



Pin Number	Name	I/O	Descriptions
1	ANT	O	Module Antenna terminal, Default terminal
2	GND	I	Ground
3	DATA	IO	Data input to be transmitted or Data pin to access the embedded EEPROM Pulled down internally to GND when configured as Transmission Enabled by DATA Pin Falling Edge and used as input pin Pulled up internally to VDD when configured as Transmission Enabled by DATA Pin Rising Edge and used as input pin
4	VCC	I	Power supply input

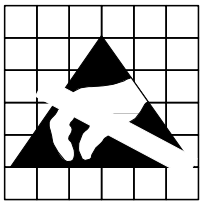
5. Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

6. Transmitter Specifications

Table 2. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}	HCT109	240		480	MHz
Synthesizer Frequency Resolution	F_{RES}	$F_{RF} \leq 480$ MHz		198		Hz
Maximum Output Power	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
PA Ramping Time[2]	t_{RAMP}		0		1024	us
Current Consumption @ 433.92 MHz	$I_{DD433.92}$	0 dBm, 50% duty cycle		6.7		mA
		+10 dBm, 50% duty cycle		13.4		mA
		+13 dBm, 50% duty cycle		17.4		mA
Sleep Current	I_{SLEEP}			20		nA
Symbol Rate	SR		0.5		30	ksps
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @ 433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-81		dBc/Hz
		200 kHz offset from F_{RF}		-83		dBc/Hz
		400 kHz offset from F_{RF}		-92		dBc/Hz
		600 kHz offset from F_{RF}		-97		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Harmonics Output for 433.92 MHz[3]	$H2_{433.92}$	2nd harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	H3	3rd harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
OOK Extinction Ration				60		dB

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. 0 and 2^n us, n = 0 to 10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

7. Typical Performance Characteristics

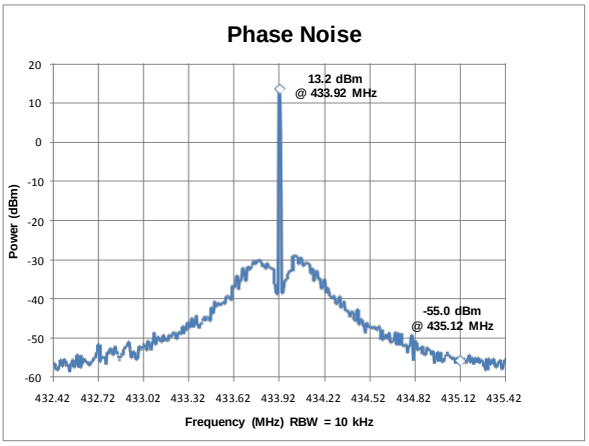


Figure 1. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

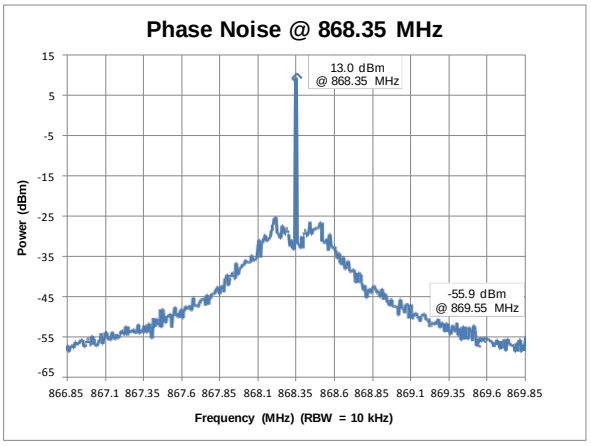


Figure 2. Phase Noise, F_{RF} = 868.35 MHz, P_{OUT} = +13 dBm, Unmodulated

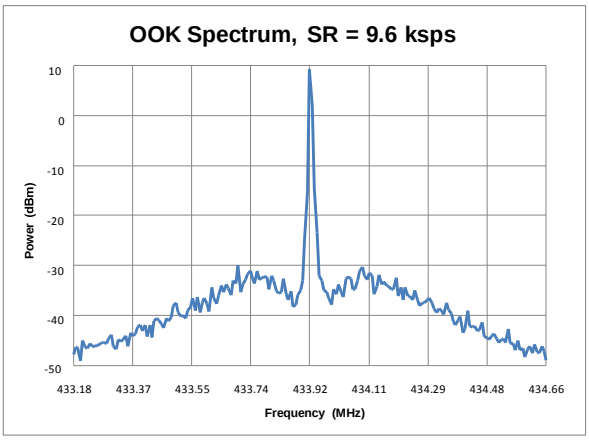


Figure 3. OOK Spectrum, SR = 9.6 ksps, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

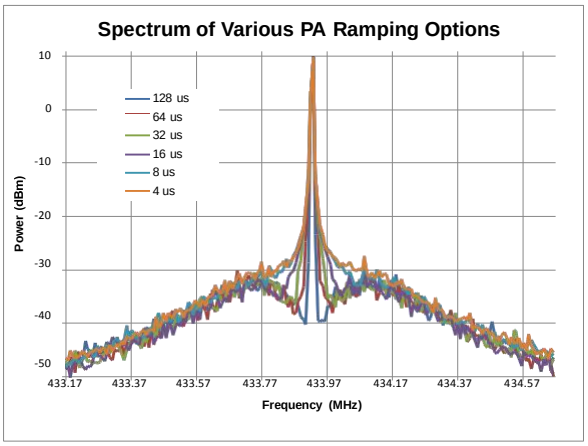


Figure 4. Spectrum of PA Ramping, SR = 9.6 ksps, P_{OUT} = +10 dBm

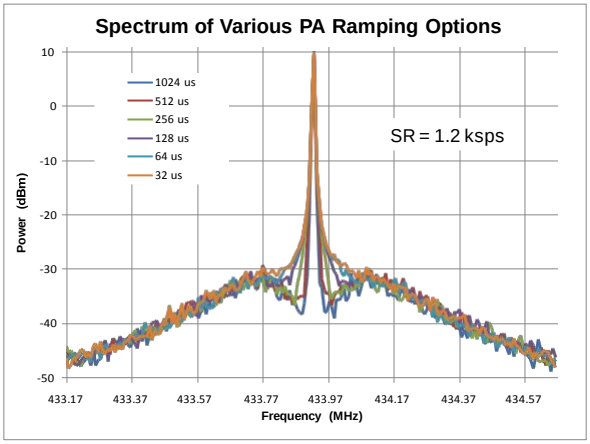


Figure 5. Spectrum of PA Ramping, SR = 1.2 ksps, P_{OUT} = +10 dBm

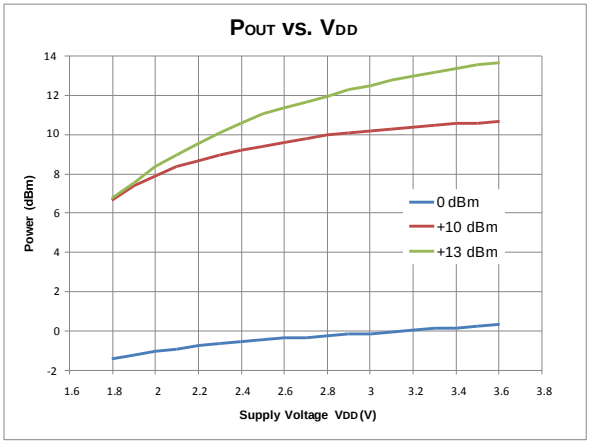


Figure 6. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

8. Functional Descriptions

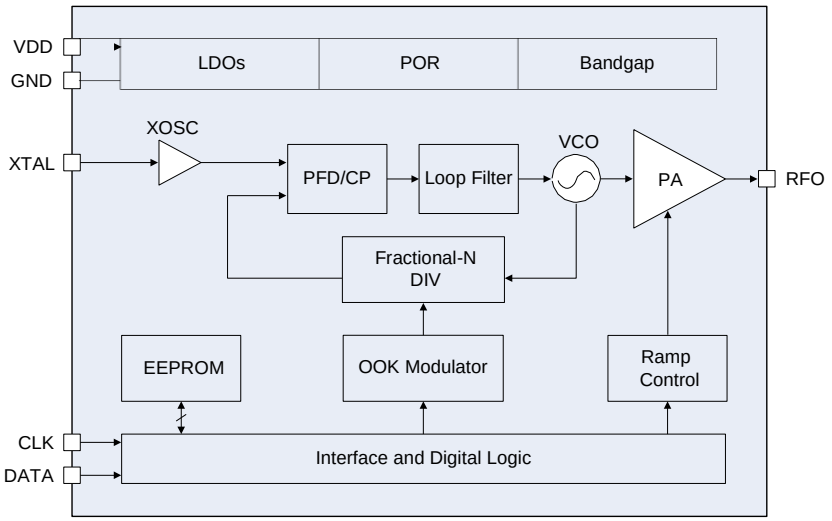


Figure 7. HC109 Functional Block Diagram

8.1 Overview

The HCT109 is an ultra low-cost, highly flexible, high performance, single-chip OOK transmitter for various 240 to 480 MHz wireless applications. The HCT109 covers the frequency range from 240 to 480 MHz . They are part of the CMOSTEK NextGenRF^{TM} family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the HCT109 is shown in the figure above. The HC109 is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the highly accurate reference voltage internally. The calibration can help the chip to finely work under different temperatures and supply voltages. The HCT109 uses the DATA pin for the host MCU to send in the data. The input data will be modulated and sent out by a highly efficient PA which output power can be configured from -10 to +13 dBm in 1 dB step size. RF Frequency, PA output power and other product features can be programmed into the embedded EEPROM by the RFPDK and USB Programmer. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock products of 433.92 MHz are available for immediate demands with no need of EEPROM programming. The HCT109 operates from 1.8 to 3.6 V so that it can finely work with most batteries to their useful power limits. Working under 3.3 V supply voltage when transmitting signal at +10 dBm power, it only consumes 13.4 mA at 433.92 MHz.

8.2 Modulation, Frequency and Symbol Rate

The HCT109 supports OOK modulation with the symbol rate up to 30 ksps. The HCT109 covers the frequency range from 240 to 480 MHz, including the license free ISM frequency band around 315 MHz and 433.92 MHz . The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz when the frequency is lower than 480 MHz, and the frequency resolution is 397 Hz when the frequency is higher than 480 MHz. See the table below for the modulation, frequency and symbol rate specifications.

Table 3. Modulation, Frequency and Symbol Rate

Parameter	Value	Unit
Modulation	OOK	-
Frequency (HC109)	240 to 480	MHz
Frequency Resolution (F_{RF} ≤ 480 MHz)	198	Hz
Symbol Rate	0.5 to 30	ksps

8.3 Embedded EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the HCT109 in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. No register access and control is required in the application program. See the figure below for the accessing of the EEPROM and Table 4 for the summary of all the configurable parameters of the HCT109 in the RFPDK.

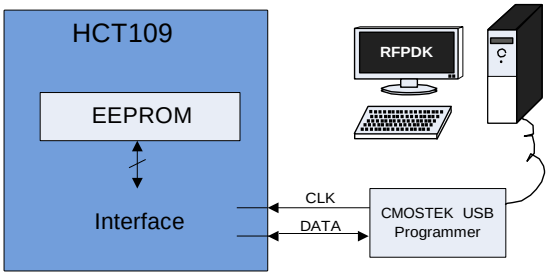


Figure 8. Accessing Embedded EEPROM

For more details of the CMOSTEK USB Programmer and the RFPDK, please refer to "AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide". For the detail of HCT109 configurations with the RFPDK, please refer to HCT109 Configuration Guideline".

Table 4. Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency (HCT109)	To input a desired transmitting radio frequency in the range from 240 to 480 MHz. The step size is 0.001 MHz.	433.92 MHz	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dBm margin is given above +13 dBm.	+13 dBm	Basic Advanced
	Xtal Cload	On-chip XOSC load capacitance options: from 10 to 22 pF.	15 pF	Basic Advanced
	PA Ramping	To control PA output power ramp up/down time, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising/Falling Edge.	Data Pin Rising Edge	Advanced
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 20 to 90 ms.	Data Pin Holding Low for 20 ms	Advanced

8.4 Power Amplifier

A highly efficient single-ended Power Amplifier (PA) is integrated in the HCT109 to transmit the modulated signal out. Depending on the application, the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application Schematic”. For the schematic, layout guideline and the other detailed information please refer to “AN101 CMT211xA Schematic and PCB Layout Design Guideline”.

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and RFPDK.

8.5 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The HC109 has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 13. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below:

$$SR_{Max} \leq 0.5 * (\frac{1}{t_{RAMP}})$$

In which the PA ramping “rate” is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by:

$$t_{RAMP} \leq 0.5 * (\frac{1}{SR_{MAX}})$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than “$0.5 * (1/SR_{Max})$”, it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to HC109 Configuration Guideline”.

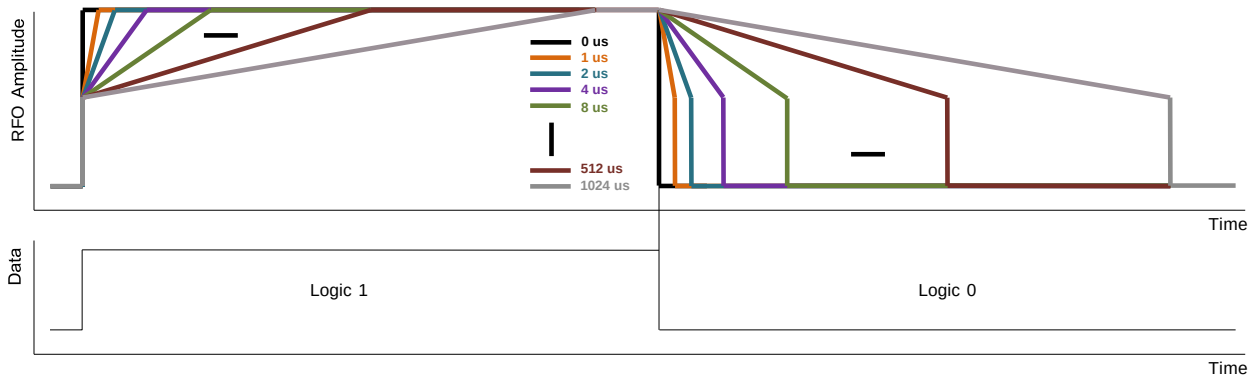


Figure 9. PA Ramping Time

8.6 Crystal Oscillator and RCLK

The HCT109 uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 10 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ù, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the HC109 to support the oscillation of the crystal.

The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency. Please refer to “AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide” for the method of choosing the right value of C_L.

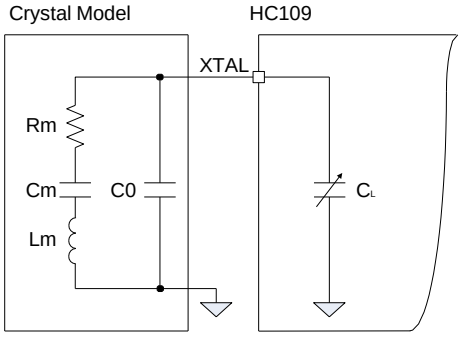


Figure 10. XTAL Circuitry and Crystal Model

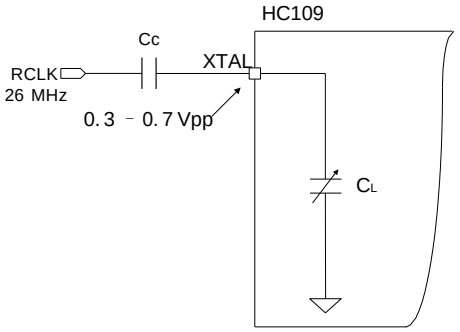


Figure 11. RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the HCT109 by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 11 for the RCLK circuitry.

9. Working States and Transmission Control Interface

9.1 Working States

The HCT109 has 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the HCT109 is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized to 20 nA typically.

XO-STARTUP

After detecting a valid control signal on DATA pin, the HC109 goes into the XO-STARTUP state, and the internal XO starts to work. The valid control signal can be a rising or falling edge on the DATA pin, which can be configured on the RFPDK. The host MCU has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in Table 5.

TUNE

The frequency synthesizer will tune the HCT109 to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the incoming data only after the TUNE state is done, before that the incoming data will not be transmitted. See Figure 12 and Figure 13 for the details.

TRANSMIT

The HCT109 starts to modulate and transmit the data coming from the DATA pin. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} can be configured from 20 to 90 ms on the RFPDK; secondly, issuing SOFT_RST command over the two-wire interface, this will stop the transmission in 1 ms. See section 6.2.3 for details of the two-wire interface.

Table 5. Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission[2]	t_{STOP}	20		90	ms
Notes: [1]. This parameter is to a large degree crystal dependent. [2]. Configurable from 20 to 90 ms in 10 ms step size.					

9.2 Transmission Control Interface

The HCT109 uses the DATA pin for the host MCU to send in data for modulation and transmission. The DATA pin can be used as pin for EEPROM programming, data transmission, as well as controlling the transmission. The transmission can be started by detecting rising or falling edge on the DATA pin, and stopped by driving the DATA pin low for t_{STOP} as shown in the table above. Besides communicating over the DATA pin, the host MCU can also communicate with the device over the two-wire interface, so that the transmission is more robust, and consumes less current.

Please note that the user is recommended to use the Tx Enabled by DATA pin Rising Edge, which is described in Section 6.2.1.

9.2.1 Tx Enabled by DATA Pin Rising Edge

As shown in the Figure 12, once the HC109 detects a rising edge on the DATA pin, it goes into the XO-STARTUP state. The user has to pull the DATA pin high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the DATA pin. The logic state of the DATA pin is “Don't Care” from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission.

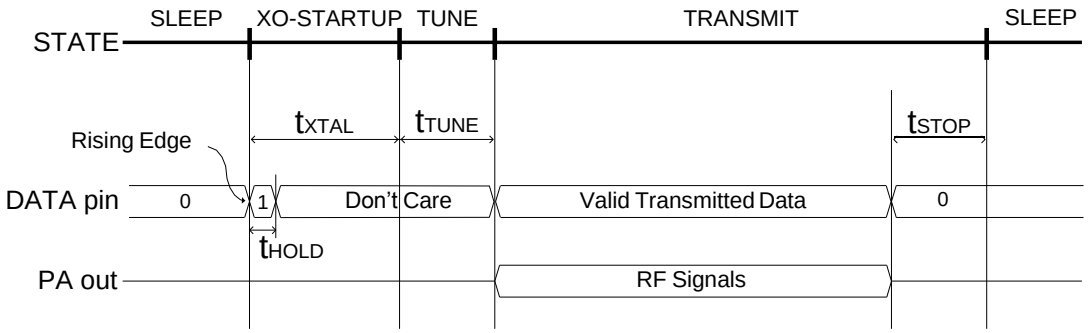


Figure 12. Transmission Enabled by DATA Pin Rising Edge

9.2.2 Tx Enabled by DATA Pin Falling Edge

As shown in the Figure 13, once the HC109 detects a falling edge on the DATA pin, it goes into XO-STARTUP state and the XO starts to work. During the XO-STARTUP state, the DATA pin needs to be pulled low. After the XO is settled, the HC109 goes to the TUNE state. The logic state of the DATA pin is “Don't Care” during the TUNE state. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission. Before starting the next transmit cycle, the user has to pull the DATA pin back to high.

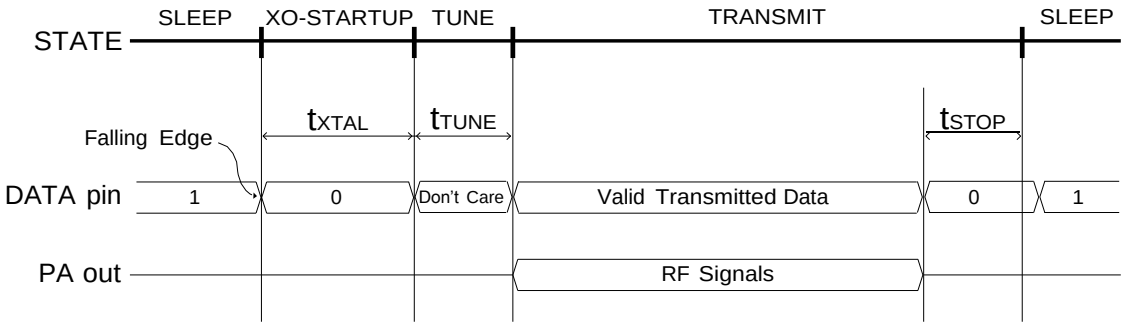


Figure 13. Transmission Enabled by DATA Pin Falling Edge

9.2.3 Two-wire Interface

For power-saving and reliable transmission purposes, the HC109 is recommended to communicate with the host MCU over a two-wire interface (TWI): DATA and CLK. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 6. TWI Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
CLK Frequency	F_{CLK}		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
CLK Delay Time	t_{CD}	CLK delay time for the first falling edge of the TWI_RST command, see Figure 20	20		15,000	ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default state			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

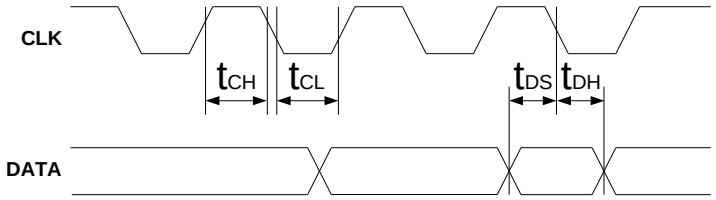


Figure 14. Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI circuit functions correctly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission. The operation flow with TWI is shown as the figure below.

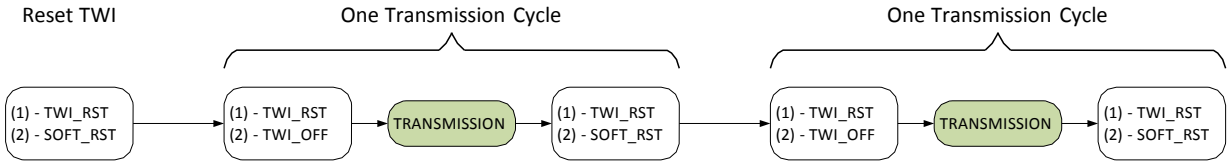


Figure 15. HC109 Operation Flow with TWI Table

14. TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the DATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The DATA pin cannot detect the Rising/Falling edge to trigger transmission after this command, until the TWI_OFF command is issued. **Notes:** 1. Please ensure the DATA pin is firmly pulled low during the first 32 clock cycles. 2. When the device is configured as Transmission Enabled by DATA Pin Falling Edge, in order to issue the TWI_RST command correctly, the first falling edge of the CLK should be sent t_{CD} after the DATA falling edge, which should be longer than the minimum DATA setup time 20 ns, and shorter than 15 us,

Command	Descriptions
	as shown in Figure 16. 3. When the device is configured as Transmission Enabled by DATA Pin Rising Edge, the default state of the DATA is low, there is no t_{CD} requirement, as shown in Figure 17.
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the DATA pin is able to detect the Rising/Falling edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 18.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 19.

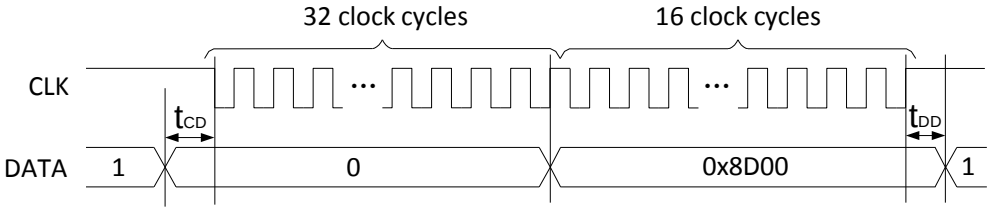


Figure 16. TWI_RST Command When Transmission Enabled by DATA Pin Falling Edge

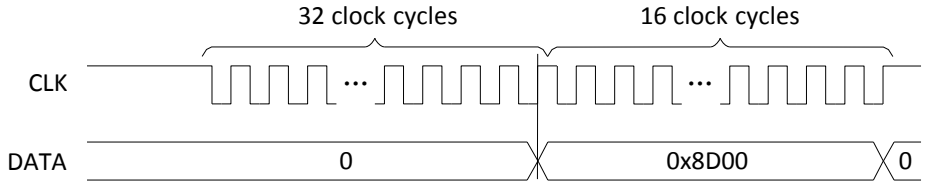


Figure 17. TWI_RST Command When Transmission Enabled by DATA Pin Rising Edge

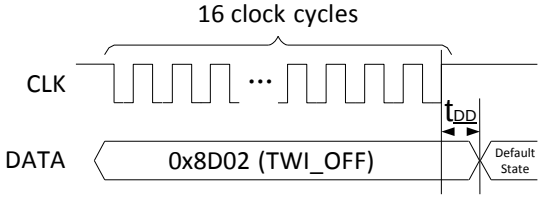


Figure 18. TWI_OFF Command

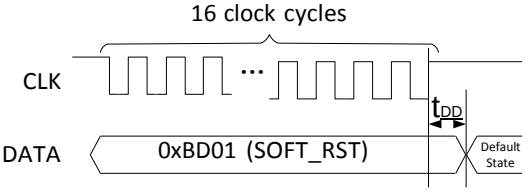
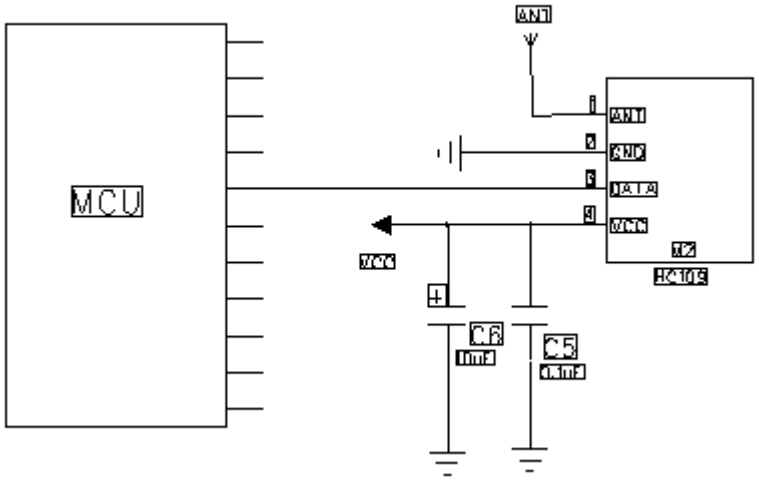


Figure 19. SOFT_RST Command

The DATA is generated by the host MCU on the rising edge of CLK, and is sampled by the device on the falling edge. The CLK should be pulled up by the host MCU during the TRANSMISSION shown in Figure 15. The TRANSMISSION process should refer to Figure 12 or Figure 13 for its timing requirement, depending on the “Start By” setting configured on the RFPDK.

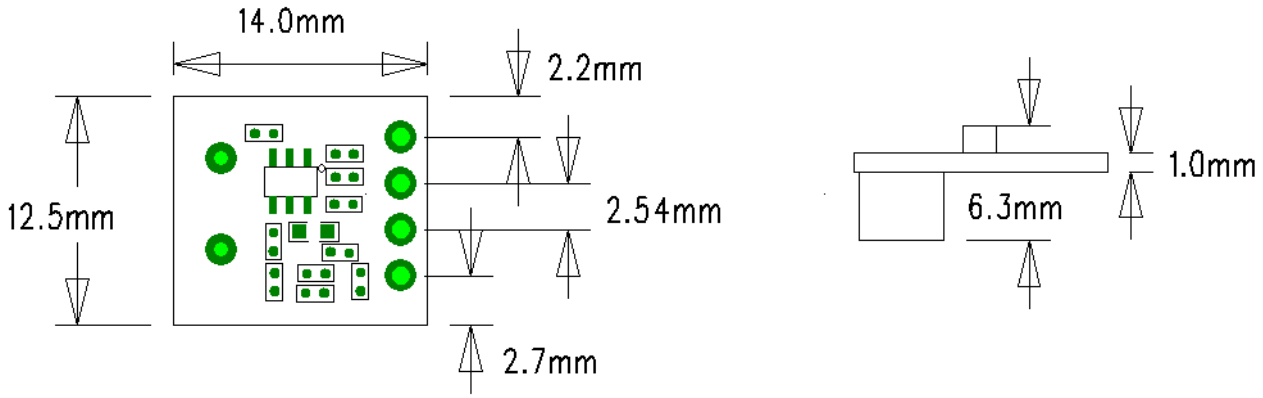
The device will go to SLEEP state by driving the DATA low for t_{STOP}, or issuing SOFT_RST command. A helpful practice for the device to go to SLEEP is to issue TWI_RST and SOFT_RST commands right after the useful data is transmitted, instead of waiting the t_{STOP}, this can save power significantly.

10. Appication



11. Module Package Outline Drawing

Unit: mm



12. Ordering Information

Part Number	Operation Band
HCT109-315	315MHz
HCT109-433	433MHz

13. Importance Notice

The HCT109 datasheet will be changed by DongGuan Holchan Electronics Technology Co.,Ltd according to the module design.

14. Contact Information

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